REMARKS

The above amendment and these remarks are responsive to the Office action of 24 Aug 2005 by Examiner Lalrinfamkim Hmar Malsawma.

Claims 1-6 are in the case.

35 U.S.C. 103

Claims 1-6 have been rejected under 35 U.S.C. 103(a) over Suzuki, U.S. Patent 5,598,029.

Applicants traverse, and argue that the Examiner has not established a prima facie case of obviousness, which requires that the Examiner provides

1. one or more references
2. that were available to the inventor and
3. that teach
4. a suggestion to combine or modify the references,
5. the combination or modification of which would appear to be sufficient to have made the claimed invention obvious to one of ordinary skill in the art.

The fourth element of the prima facie case, the suggestion to combine, must come from the prior art. It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements. [See Arkie Lures, Inc. v. Gene Larew Tackle, Inc., 43 USPQ 2d 1294 (Fed. Cir. 1997)]. That a claimed invention may employ known principles does not itself establish that the invention would have been obvious, particularly where those principles are employed to deal with different problems. The Examiner must consider the claim as a whole, and not piece together the claimed invention using the claims as a guide. The Federal Circuit has stated: "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. [See In re Fritch, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992)].

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). To reach a conclusion of obviousness under § 103, the Examiner must produce a factual basis supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Such evidence is required in order to establish a prima facie case. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). The Examiner must not only identify the elements in the prior

art, but also show 'some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead the individual to combine the relevant teachings of the references. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

A rejection under 35 U.S.C. § 103 must be based on whether there is a teaching, motivation, or suggestion to select and combine the references based on objective evidence of record. Therefore, the Examiner must identify a reason, suggestion, or motivation which would have led an inventor to combine those references. Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1629, (Fed. Cir. 1996).

With respect to the present application, applicants note that Suzuki is describing a layout which is significantly different from that described by applicants, and cannot be applied consistent with respect to the above considerations to applicant's claims.

Suzuki is describing an NFET tied as a capacitor. The layout as shown in Figure 4 shows a **p-type substrate** 20 with a source/drain region 8 that is n-type (specified in column 5 lines 4-6 of Suzuki). the source/drain regions are connected to GND and the gate 4 is connected to the power source. This causes an inversion layer to be created, pulling the **minority** carriers to the surface of the

substrate underneath the gate oxide 3.

This is different from applicant's invention, which does not use normal MOSFETsd tied in this manner. Applicant's PCAPs have a "source"/"drain" region that is n-type (or have P doping) inside of a P-type substrate (or P-well). With the gate tied to the ground and the "source" and "drain" regions tied to the power supply, the **majority** carriers accumulate at the surface of the substrate underneath the gate oxide. Similarly, as will be apparent to those of skill in the art, a source/drain region that is n-type (or have N+ doping) inside an n-type substrate (or N-well) could be used. In either configuration, there is no inversion layer. The differences in these configurations result in a higher capacitance than a same size NFET configuration as shown by Suzuki.

Applicants have amended claim 1 to point out this feature, support for which is found in Figure 10, showing majority carriers forming in diffusion layer 150 underneath the gate oxide insulator. There is no inversion layer in the structure shown in Figure 10, thus providing support for the negative limitation added to claim 1.

This is significant in the context of the Examiner's statement that in the event of a gate oxide defect, there is still a resistive path due to the inversion layer. [Office Action, page 3.] Applicants traverse that statement, for it

goes completely against the whole concept of how a FET works. By applying the correct gate voltage, a **highly conductive** inversion layer is created along the surface of the substrate that allows for current conduction from the source to the drain. In the example specified by Suzuki, that inversion layer does exist. So it would be a simple matter to short the power supply on the gate to the grounded source/drain regions through a defect in the gate oxide, and Suzuki's capacitor does not, as the Examiner states at page 4 of the Office Action, "...provide a structure comprising contacts being located and capable of limiting defect current while suppressing noise".

Accordingly, applicants argue that Suzuki does not teach:

> "...protecting surrounding circuits in the event there is a defect shorting said busses together by limiting defect current while allowing said capacitor to function at a frequency sufficiently high to suppress noise on said first and second busses to a value which achieves bus stability..."

As argued in their response to the previous Office Action, regarding claim 1, the Examiner rejects the claim because Suzuki shows a method for wiring the decoupling capacitor to the power supply lines. However, the method proposed by Suzuki expressly limits the parasitic resistance

due to the wiring method (column 3, lines 54 - 56 and column 4, lines 4 - 7). The fixed resistance formed by the contacts is purely due to the number of contacts used.

> "The parasitic resistance can be suppressed small by shortening the length and thickening the width of the electrode of the bypass capacitor... Further, since the value of the parasitic resistance which is connected to the bypass capacitor is small, the effect of eliminating the power supply noise is great." [Suzuki, Col. 3, lines 54-56, and Col. 4, lines 4-7.]

Applicants purposely add parasitic [to use Suzukik's term] resistance [that is, in Applicants' terminology, fixed resistance formed by contacts connecting the polysilicon layer to a first voltage level buss and the diffusion layer to a second voltage level buss] to protect surrounding circuits in the event there is a defect shorting the VDD and GND plates together. The current draw through the defect in the event of a short would render the chip useless. Also, the resistance added is due to where the contacts are placed and not how many contacts are used.

The Examiner points out that the term "sufficiently high" is relative. That would be true, but for the fact that Applicants' claims clearly recite exactly how high is sufficient. That is, the term "sufficiently high" is qualified by the phrase "...to suppress noise on said first and second busses to a value which achieves bus stability".

Those of skill in the art understand that placement (location, separation) of the contacts to achieve the result of bus stability and noise suppression is dependent upon structural and circuit parameters which in any particular configuration may be determined with reference to the claims and specification without undue experimentation.

Regarding dependent claims 2-6, Applicants purposely add resistance, whereas the parasitic resistance in the design described by Suzuki is negligible. Applicants' design allows the protection resistance to be built into the layout of the capacitor without adding a discrete resistor element in series with the capacitor to the layout. If there is a short between the VDD and GND plates, Applicants' design would have the same current-limiting ability as a prior art design that would include a discrete resistor element. However, in such a design, that resistance is there whether or not the leakage protection is required. The calculation of the RC factor that determines the noise suppression ability of the decoupling capacitor in Applicants' design would use a resistance value half that of the protection resistance. This means Applicants' design is able to suppress more noise than a prior art design that includes a discrete resistor element.

This is why Applicants' claims include the RC factor, the bandwidth limiting resistance VS the leakage protection resistance, etc.

Because Applicants are purposely adding resistance, the design is very different from the one described by Suzuki. The design described by Suzuki would never be able to do any of this because he is trying to minimize the parasitic resistance. There is no protection if his VDD and GND plates were to short together, due to the presence of the highly conductive inversion layer, as previously discussed.

Consequently, Applicants argue, Suzuki teaches away from the invention described and claimed by Applicants, and does not contain "all pertinent structural limitations necessary for one of ordinary skill in the art to attribute the generalized features recited in the instant claims." [Office Action, page 6.]

The Examiner objects to the use of relative, non-specific limitations in the claims [Office action, page5], and kindly suggests several structural limitation that could be added to the claim [Office action, page 7].

With respect to the features listed as "relative terminology", applicants argue that circuit designers of ordinary skill in the art will recognize that these features are technology dependent (as applicants teach in their specification at pages 18:7 and 19:3-5), and that the specific values may be calculated from the teachings of applicants as they may apply to a particular current or future technology. Applicants provide teachings sufficient to calculate the various design parameters called for in the

claims at, for example, pages:lines 13:9-14, 14:1-8, 16:15 to 17:2, 17:13 to 18:2, and 18:12 to 19:8.

With respect to the current limiting resistance (R), in the Cu11 and Cu08 technologies, 50 ohms is used. However, this is technology dependent, and specified by the technologists who develop each technology node. Applicant's bandwidth limiting resistance (the resistance used to calculate the highest frequency noise that can be suppressed on the power busses) is set to half of the current limiting resistance (R/2) by design. For future technology nodes, the current limiting resistance to be designed into the capacitor may go up or down as necessary, and may need to be designed with a specific noise frequency in mind. These variations are technology dependent, and are not appropriately limiting features in claims directed to applicant's invention.

With respect to sheet resistance, the Examiner states, "...i.e., since the 'sheet resistance' has not been quantified and therefore could be of any value, '10% of any value' is essentially 'any value' that one chooses." Applicants traverse. The sheet resistance is specified by the technologists who develop each technology node. It changes from one technology to the next, but is precise for a given technology. For example, for technology Cu11, the nominal sheet resistance of diffusion is 7 ohms per square. For technology Cu08, that changed to 8 ohms per square. Applicants could not possibly define a specific value in

anticipation of all possible technologies that could take advantage of applicant's invention.

With respect to location of contacts, applicants provide teachings adequate to those of skill in the art to locate the contacts in accordance with the limitations of the claims. There are many variables which the designer will consider, including the current limiting resistance specified for the reliability required for a particular circuit, the sheet resistance of the polysilicon and diffusion layers specified in the design manual for each technology, the desired dimensions of the capacitor required for a particular application. The derivation of the location of contacts in accordance with the parameters set forth in the claims is what applicants have taught those of ordinary skill in art to do.

Applicants urge that claims 1-6 be allowed.

SUMMARY AND CONCLUSION

Applicants urge that the above amendments be entered and the case passed to issue with claims 1-6.

The Application is believed to be in condition for allowance and such action by the Examiner is urged. Should

differences remain, however, which do not place one/more of the remaining claims in condition for allowance, the Examiner is requested to phone the undersigned at the number provided below for the purpose of providing constructive assistance and suggestions in accordance with M.P.E.P. Sections 707.02(j) and 707.03 in order that allowable claims can be presented, thereby placing the Application in condition for allowance without further proceedings being necessary.

Sincerely,

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By

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